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| First Named Inventor | Pankaj Kedia |
| Art Unit | 2116 |
| Examiner Name | Chen, Tse W. |
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  - ☐ Affidavits/declaration(s)
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Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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| Signature | [signature] III |
| Date | April 14, 2008 |

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re the Patent Application of:

Pankaj Kedia

Serial No.: 09/753,326

Art Unit: 2116

Filed: December 29, 2000

Examiner: Chen, Tse W.

For: Low Power Subsystem For Portable Computers

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

REPLY
TO THE EXAMINER'S ANSWER IN THE ABOVE-CAPTIONED APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellant") hereby submit this Reply in further support of its appeal from a final decision by the Examiner, mailed August 31, 2007 in the above-captioned case. The Examiner provided an Answer mailed February 25, 2008.

An oral hearing is not desired.

## I. ALLOWED CLAIMS ?

In the Answer, the Examiner did not reiterate in Section 9 any of the rejections against the following claims: 30, 33-37, 41, 43, 45-47, 53-56. The Examiner also made no indication of the status of these claims. Without any statement about these claims in the Answer, Appellant must assume that the rejections are withdrawn and that these claims are allowed.

## II. RESPONSE FOR CLAIM 29

As to Claim 29, the Examiner maintains the same Umina, Barber obviousness rejection and provides some more information about this rejection in the Response to Arguments.

### A. Components of the Low Power Subsystem

The Examiner begins the response with "Applicant argues that 'neither reference shows a whole subsystem' but does not point out which claimed limitation relating to the subsystem is missing from the combined references." Claim 29 recites, "the low power subsystem including a low power processor, an external interface and a low power memory."

Both references have two processors, but in Umina both are high power, high speed processors. In Barber, there is a high power processor and a low power processor.

#### i. Low Power Memory

Neither reference shows an external interface, nor a low power memory. As explained previously, neither reference shows a separate external interface as part of a low power subsystem. Barber's external interface 48 is shared and used in both modes. Umina lacks a system level diagram, but there would be no reason to expect a separate low power interface nor any separate external interface in a system with no low power mode. As to the low power memory, Umina has a second memory but it is a high speed,

high power memory. Barber has a single shared memory, which, accordingly, would also be a high speed, high power memory.

As for the ***claimed*** limitations missing from the ***combined*** references (Examiner's emphasis), if neither reference shows the claimed low power memory, nor the external interface, then the combined references do not show it either.

The Examiner argues that the ***combination*** shows that it would be "obvious to incorporate Barber's low power operation mode associated with dual processor into Umina's own dual processors system in order to conserve power consumption." Ignoring the matter of the missing external interface for now, at the time of Barber's filing in 1998, dual processor, dual memory systems had been known for years. These systems generally would share a hard drive and then the SRAMs would be used for short term and immediate storage. Managing the SRAMs was always complicated and so it was also known to use a single SRAM shared by two processors. Dual processor systems were generally adopted to increase the processing power.

While with hindsight Barber could have used two memories, for the system in the cited reference, Barber nevertheless chose to use a single SRAM. The references do not show a second low power memory, but instead dual memories are used for higher speed when higher power consumption is not a concern. Most likely, Barber does not use a second memory because Barber is not trying to increase processing speed. Barber is trying to reduce power consumption. The cited prior art does not show that adding another memory will reduce power consumption. Instead, the prior art shows that a second memory increases speed, power consumption and memory management overhead.

To adapt Barber using Umina to achieve the Claim 29 invention (setting aside the external interface issue) would require first that Barber look at high speed, high power, high cost systems like Umina for inspiration. Next, it would require adding the second SRAM and all of the additional memory management overhead from Umina, adding

further cost and complexity and reducing the power savings. Then, it would require that the SRAM be changed to a low power memory type (not in either reference). Finally, it would require that Barber be adapted to be able to access data contained within the main processor SRAM or other memory when the main CPU is in low power mode (also not in either reference, since Barber has just the one memory). The Examiner has not provided a motivation for adding another memory from Barber, just so that the low power processor can access the original memory.

Appellant submits that it would not be obvious to modify Umina with the teachings of Barber since Umina is directed to high speed, high cost systems and swapping one of the CPUs with a low power processor would seriously degrade performance.

In fact, Barber's system is just like a conventional single processor system except for the addition of a low power processor. Barber switches over to the low power processor for the low power mode. This avoids all of the complication of sharing SRAM, saving states, etc. that are mentioned, for example in Umina.

**ii. <u>External Interface</u>**

The Examiner next responds to the issue of the ***<u>separate</u>*** external interface (Examiner's emphasis). Appellant respectfully submits that claim 29 recites a "low power subsystem including... an external interface." The Examiner may perhaps be surmising that while it is included in the low power subsystem, the same external interface may also be included in the main computer system. The claim was not intended for such an interpretation and the preferred embodiments of the specification do not suggest such an implementation. However, if the Board finds the claim to be ambiguous, then Appellant is willing to amend the claim on that point.

**iii. <u>Subsystem</u>**

The Examiner also responds that Umina and Barber show a low power subsystem. Umina, of course, does not show a low power anything, but a high speed, high power

system. The processors each have an SRAM, but the SRAMs can be swapped between the processors so that it is also difficult to say that one pairing belongs to one subsystem as anything other than a transient current operational mode. Barber shows two processors that share all of the other resources. The Examiner points to the external interface 48 as part of the low power subsystem, but it is clearly a shared resource that is used by either processor in either mode.

### B. <u>Combining the References</u>

The Examiner responds that modifying Umina as proposed by the Examiner does not go against Umina at Col. 1, lines 50-65 since that section is about the ***<u>prior art</u>*** (Examiner's emphasis). The Examiner is correct that Appellant cited the prior art section of Umina. In this section, Umina explains that the Figure 1 kind of dual processor/dual SRAM system has drawbacks: 1) inefficiency; 2) limited data transfer rates; and 3) complex programming to avoid inadvertent overwrites. Umina strives to improve upon this with higher speed, reliability, and simpler programming. As Appellant explained in the Appeal Brief, the modification that the Examiner suggests would be to change Umina to more closely resemble its Figure 1 approach, which Umina expressly rejects. Appellant is merely arguing that it is not obvious to adapt the teachings of a reference to more closely resemble the prior art that the same reference rejects.

The Examiner starts the Response for Claim 29, with "Applicant's individualistic analysis of the reference does not clarify the rejection based on combination." Appellant replies that when elements are missing from both references (low power memory, low power subsystem with the memory and an external interface, providing accessed data through the low power subsystem external interface, accessing data in the other memory from the low power processor when the high power CPU is in low power mode) then the combination does not render the claim obvious. In such a case, it is appropriate to first examine each reference individually.

The Examiner also states in the Response for Claim 29 that "In other words, Umina discloses the main structural components, including operations such as using one processor [206] to access data within the computer system memory [204] during normal operation, but did not discuss other operation modes such as low power operation. Thus, Examiner provided Barber, which also discloses a dual processor system, to disclose the low power operation." While Barber does indeed show low power operation with the additional processor, Barber adds nothing about how to manage two memories, nor a low power subsystem external interface.

In sum, there are features absent in both references. Even if the combination were obvious, such a combination could not meet the claim. In addition, there is difficulty in adapting the features of one reference into the other even ignoring the missing features.

## III. RESPONSE FOR CLAIM 30

In Kableshkov Figure 2, a host processor 30 and a coprocessor 40 both have independent access to a relational database stored on a hard disk 34 through a common I/O bus 32. The reference does not say whether the co-processor also has memory, however, the co-processor has access to the host processor's local cache memory 31. The Examiner relies heavily on the idea that the data in the local cache memory is a relational database. The section of the reference cited in the Answer states "a copy of the database or part thereof residing in a main memory 31 of the host processor 30." The reason that the local cache contains a database or part thereof is that the hard disk contains a database and the whole purpose of the system is to operate on that database.

The first difference between this and Claim 30 is first that the shared database in Claim 30 is "of the low power subsystem." In Kableshkov, the shared database is the cache of the main processor. The second difference is that in Claim 30 a partial copy of the computer system memory is stored in the shared database. In Kableshkov, the

computer system memory itself is used. The third difference is that the data on the computer system memory of Claim 30 does not have to be a database.

The Examiner suggests that Kableshkov suggests accessing data at the co-processor through a shared database. To the person of average skill, the context of this suggestion is important. In Kableshkov, all the data is a database, so Kableshkov would not suggest using a partial copy of a database to access other types of data, it would only suggest having a local cache of the type of data that is on the hard disk. While the co-processor can access the host processor's local cache, this is no different from any other dual processor or co-processor system in which there is a single SRAM local cache used by both processors. The reference is further from the current invention even than Barber in which the processors act independently.

## IV. RESPONSE FOR CLAIMS 38 AND 51

In the Answer's Response section for Claims 38 and 51, the Examiner makes a curious objection to Appellant's explanations by calling them not logical or questionable. It is not Appellant's logic that is at issue, but the teachings of the references, in this case Hollon. Hollon provides the advantage that the computer can be operated with the lid closed. For anyone that has tried to use a notebook computer quickly or in close quarters, the benefit is clear. While Hollon does not address power consumption except generally in the Background section, Appellant acknowledges that the power consumed by the main display might be more than that consumed by the mini-display and ASIC combined. In such a case the lid closed mode might be a lower power mode than the lid open mode. None of this pertains to how the rejection is insufficient to invalidate the claims.

More seriously, the Examiner has dismissed Appellant's explanation of the operation of the CPU, ASIC, memory, etc in Hollon. The operation of the system is clearly shown in the figures by the reference numbers referenced by Appellant in the

Appeal Brief. As additional support Appellant refers to "ASIC 84 coordinates with video control 83" (Col. 3, ll. 37-38) meaning that both are operating simultaneously.

Figure 9 shows "Keyboard controller 92 respectively maps spontaneous use function keys 31-38 to function keys 11 through 18" (Col. 3, ll. 57-59) "[K]eyboard controller is connected to system bus 80 through an input/output (I/O) controller 91." These statements together mean that the keyboard controller, system bus and I/O controller are also operating in the spontaneous use mode. A closer reading of these sections reveal that the purpose of the ASIC is not to take over for the CPU. It is an auxiliary display controller (Col. 3, ll. 35-41) that maps pixels generated by the video controller onto the mini-display. Hollon does not describe any other function for the ASIC.

Even if it may seem illogical or questionable, Hollon's system uses all of the system resources (except the main display) including the main video controller and CPU when in the spontaneous use mode. While Hollon at Col. 3, ll.1-5 describes putting the computer into "inactive mode" before closing the lid, there is no indication that the computer can be active in the inactive mode. Pressing a spontaneous use key "activates spontaneous use display," but it must also activate the video controller, and as explained above, the CPU, system bus and the main memory. Hollon in no way suggests that the computer stays in its inactive mode after the spontaneous use display is activated and it is difficult to understand how the system can operate without its CPU and main memory. If the Examiner can make a showing based on the reference of how that might be, then Appellant would be interested in seeing that. So far however, no such showing has been made.

The remainder of the Examiner's Answer is not clearly understood. Appellants note that the rejection relies on Hollon having a low power subsystem that operates when the CPU is in a low power mode. As can be seen in Figure 8 of Hollon, there is no low power subsystem with a low power processor and low power memory. There is an ASIC

that operates as a display adapter and there is a second display. The ASIC operates with the CPU active.

As with the other rejections, there are significant elements in the rejected claims that are not shown in the cited references. In all of the rejections, the Examiner has yet to find a low power subsystem that consists of any more than a sole processor. The addition of the low power memory and external interface provide significant benefits. The addition of access to the main memory while the CPU is in a low power mode adds even further benefits. These are not only new but not obvious from any of the references.

## VIII. <u>CONCLUSION</u>

Appellant respectfully submits that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: April 14, 2008

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